

Abstract of the Disclosure

A method for fabrication of silicon-on-nothing (SON) MOSFET using selective etching of  $\text{Si}_{1-x}\text{Ge}_x$  layer, includes preparing a silicon substrate; growing an epitaxial  $\text{Si}_{1-x}\text{Ge}_x$  layer on the silicon substrate; growing an epitaxial thin top silicon layer on the epitaxial  $\text{Si}_{1-x}\text{Ge}_x$  layer;

5      trench etching of the top silicon and  $\text{Si}_{1-x}\text{Ge}_x$ , into the silicon substrate to form a first trench; selectively etching the  $\text{Si}_{1-x}\text{Ge}_x$  layer to remove substantially all of the  $\text{Si}_{1-x}\text{Ge}_x$  to form an air gap; depositing a layer of  $\text{SiO}_2$  by CVD to fill the first trench; trench etching to from a second trench; selectively etching the remaining  $\text{Si}_{1-x}\text{Ge}_x$  layer; depositing a second layer of  $\text{SiO}_2$  by CVD to fill the second trench, thereby decoupling a source, a drain and a channel from the substrate; and

10     completing the structure by state-of-the-art CMOS fabrication techniques.